

1 CLAIMS:

2 1. A method of forming a dynamic random access memory
3 (DRAM) comprising:

4 forming an insulative layer over a substrate having a plurality of
5 conductive lines which extend within a memory array area and a
6 peripheral area outward of the memory array; and

7 contemporaneously etching capacitor container openings over the
8 memory array and contact openings within the insulative layer over
9 conductive line portions within the peripheral area.

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11 2. The method of claim 1, wherein the etching of the capacitor
12 container openings and contact openings comprises etching said openings
13 to have substantially the same opening dimensions.

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15 3. The method of claim 1, wherein the etching of the capacitor
16 container openings and contact openings comprises exposing insulative
17 cap portions of conductive lines in the peripheral area.

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19 4. The method of claim 1, wherein the etching of the capacitor
20 container openings and contact openings comprises exposing insulative
21 cap portions of conductive lines in both the memory array area and the
22 peripheral area.

1 5. The method of claim 1, wherein the etching of the capacitor
2 container openings and contact openings comprises:

3 etching said openings to have substantially the same opening
4 dimensions; and

5 exposing insulative cap portions of conductive lines in the
6 peripheral area.

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8 6. The method of claim 1 further comprising after the etching,
9 contemporaneously forming conductive material within the capacitor
10 container openings and contact openings, the conductive material within
11 the capacitor container openings comprising at least a portion of a
12 capacitor electrode layer.

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14 7. The method of claim 1 further comprising patterning and
15 removing conductive cell plate material within the memory array, said
16 removing also removing conductive material from within said contact
17 openings over said conductive line portions.

1 8. The method of claim 1 further comprising after the etching:
2 contemporaneously forming conductive material within the capacitor
3 container openings and contact openings, the conductive material within
4 the capacitor container openings comprising at least a portion of a
5 capacitor electrode layer; and

6 removing the conductive material from within the contact openings
7 within the peripheral area and removing portions of an overlying
8 insulative cap from over the conductive line portions to expose
9 conductive material of the conductive lines within the peripheral area.

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11 9. The method of claim 1 further comprising after the etching:
12 contemporaneously forming conductive material over the substrate
13 and within the capacitor container openings and contact openings, the
14 conductive material within the capacitor container openings comprising
15 at least a portion of a capacitor electrode layer;

16 removing the conductive material from within the contact openings
17 within the peripheral area and removing portions of an overlying
18 insulative cap from over the conductive line portions to expose
19 conductive material of the conductive lines within the peripheral area;
20 and

21 after the removing, forming additional conductive material over and
22 in electrical communication with the conductive line portions.

1 10. A method of forming a dynamic random access memory
2 (DRAM) comprising:

3 forming an insulative layer over a substrate having a plurality of
4 conductive lines which extend within a memory array area and a
5 peripheral area outward of the memory array; and

6 in a common photomasking step, etching capacitor container
7 openings over the memory array and contact openings over conductive
8 line portions within the peripheral area.

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10 11. The method of claim 10, wherein the etching of the
11 capacitor container openings and the contact openings comprises
12 contemporaneously etching at least portions of the openings.

1 12. A method of forming a dynamic random access memory
2 (DRAM) comprising:

3 forming a patterned masking layer over a substrate having a
4 plurality of openings formed within an insulative layer, some of the
5 openings comprising capacitor container openings within a memory array
6 and having at least a portion of a capacitor electrode layer disposed
7 therein, other of the openings comprising conductive line contact
8 openings disposed over conductive lines within a peripheral area outward
9 of the memory array; and

10 with said common patterned masking layer, removing unmasked
11 portions of the capacitor electrode layer within the memory array, and
12 removing material from over portions of the conductive lines within the
13 peripheral area sufficient to expose conductive material of the conductive
14 line portions.

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16 13. The method of claim 12, wherein the removing of the
17 material from over portions of the conductive lines within the peripheral
18 area comprises removing conductive material from which the capacitor
19 electrode layer was formed.

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21 14. The method of claim 12, wherein the removing of the
22 material from over portions of the conductive lines within the peripheral
23 area comprises removing insulative cap portions from over the
24 conductive line portions.

1 15. The method of claim 12, wherein the removing of the
2 material from over portions of the conductive lines within the peripheral
3 area comprises removing insulative cap portions comprising a nitride
4 material from over the conductive line portions.

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6 16. The method of claim 12, wherein the removing of the
7 unmasked portions of the capacitor electrode layer and the removing of
8 the material from over portions of the conductive lines within the
9 peripheral area comprises contemporaneously removing conductive
10 material from within the memory array and from within the contact
11 openings within the peripheral area.

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13 17. The method of claim 12, wherein the removing of the
14 material from over portions of the conductive lines within the peripheral
15 area comprises removing first and second conductive materials from over
16 the conductive line portions.

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18 18. The method of claim 12, wherein the removing of the
19 material from over portions of the conductive lines within the peripheral
20 area comprises removing first and second conductive materials from over
21 the conductive line portions, the first and second conductive materials
22 being elevationally spaced apart and separated by an intervening
23 dielectric region.

1 19. A method of forming a dynamic random access memory
2 (DRAM) comprising:

3 forming a plurality of conductive lines over a substrate having a
4 memory array area and a peripheral area outward of the memory array
5 area, the conductive lines having an insulative material layer formed
6 thereover;

7 forming a storage capacitor electrode layer over the substrate; and
8 using a common etch chemistry, removing material of the
9 insulative material layer and material of the storage capacitor electrode
10 layer within the peripheral area.

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12 20. The method of claim 19, wherein no material of the storage
13 capacitor electrode layer within the memory array area is removed
14 during said removing.

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16 21. The method of claim 19, wherein the insulative material
17 comprises individual insulative material caps over the conductive lines.

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19 22. The method of claim 19, wherein:

20 the insulative material comprises individual insulative material caps
21 over the conductive lines; and

22 the removing of the material of the insulative material layer
23 comprises removing insulative material cap portions from over conductive
24 lines in the peripheral area.

1 23. The method of claim 19, wherein the insulative material
2 layer comprises a first insulative material layer and further comprising
3 prior to the forming of the storage capacitor electrode layer,
4 contemporaneously forming openings within a second insulative material
5 layer over the conductive lines within the peripheral area and the
6 memory array area, the openings over the peripheral area as initially
7 formed exposing the first insulative material layer but not conductive
8 material of the conductive lines.

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10 24. The method of claim 19, wherein the insulative material
11 layer comprises first insulative material layer caps over the conductive
12 lines, and further comprising prior to the forming of the storage
13 capacitor electrode layer, contemporaneously forming openings within a
14 second insulative material layer over the conductive lines within the
15 peripheral area and the memory array area, the openings over the
16 peripheral area as initially formed exposing the first insulative material
17 layer but not conductive material of the conductive lines.

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19 25. The method of claim 19, wherein the insulative material
20 comprises silicon nitride and the capacitor electrode layer comprises a
21 conductively doped silicon.
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1 26. A method of forming a dynamic random access memory
2 (DRAM) comprising:

3 forming a plurality of conductive lines over a substrate having a
4 memory array area and a peripheral area outward of the memory array
5 area, the conductive lines having an insulative material layer formed
6 thereover;

7 forming a storage capacitor storage node electrode layer over the
8 memory array and the peripheral area; and

9 contemporaneously removing material of the insulative material
10 layer and material of the storage capacitor storage node electrode layer
11 within the peripheral area.

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13 27. A method of forming a dynamic random access memory
14 (DRAM) comprising:

15 forming a plurality of conductive plugs received over substrate
16 node locations over which storage capacitors are to be formed within
17 a memory array area; and

18 after the forming of the plugs, removing insulative material over
19 and exposing conductive material of conductive lines which are formed
20 within a peripheral area outward of the memory array area, said
21 exposing being a first-in-time exposure of conductive material of the
22 conductive lines in the peripheral area after provision of said insulative
23 material thereover.

1 28. The method of claim 27, wherein the insulative material
2 comprises a first insulative material, and further comprising prior to the
3 removing of the first insulative material, forming capacitor container
4 openings within a second insulative material over conductive lines within
5 the memory array area.

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7 29. The method of claim 27, wherein the insulative material
8 comprises a first insulative material, and further comprising prior to the
9 removing of the first insulative material, contemporaneously forming both
10 capacitor container openings within a second insulative material over
11 conductive lines within the memory array area, and contact openings
12 within the second insulative material over the conductive lines within the
13 peripheral area.

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15 30. The method of claim 27, wherein the insulative material
16 comprises a first insulative material, and further comprising prior to the
17 removing of the first insulative material:

18 contemporaneously forming both capacitor container openings within
19 a second insulative material over conductive lines within the memory
20 array area, and contact openings within the second insulative material
21 over the conductive lines within the peripheral area; and

22 forming a capacitor electrode layer within the capacitor container
23 openings and the contact openings.
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1 31. The method of claim 27, wherein the insulative material
2 comprises a first insulative material, and further comprising prior to the
3 removing of the first insulative material:

4 contemporaneously forming both capacitor container openings within
5 a second insulative material over conductive lines within the memory
6 array area, and contact openings within the second insulative material
7 over the conductive lines within the peripheral area; and

8 forming a pair of capacitor electrode layers and an intervening
9 dielectric region therebetween within the capacitor container openings
10 and the contact openings.

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12 32. The method of claim 27, wherein the insulative material
13 comprises a first insulative material, and further comprising prior to the
14 removing of the first insulative material:

15 contemporaneously forming both capacitor container openings within
16 a second insulative material over conductive lines within the memory
17 array area, and contact openings within the second insulative material
18 over the conductive lines within the peripheral area;

19 forming a capacitor electrode layer within the capacitor container
20 openings and the contact openings; and

21 removing the capacitor electrode layer from within the contact
22 openings and not from within the capacitor container openings.

1 33. The method of claim 27, wherein the insulative material
2 comprises a first insulative material, and further comprising prior to the
3 removing of the first insulative material:

4 contemporaneously forming both capacitor container openings within
5 a second insulative material over conductive lines within the memory
6 array area, and contact openings within the second insulative material
7 over the conductive lines within the peripheral area;

8 forming a capacitor electrode layer within the capacitor container
9 openings; and

10 wherein the removing of the first insulative material comprises
11 using an etch chemistry effective to remove both the first insulative
12 material and selected portions of the capacitor electrode layer over the
13 memory array.

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15 34. The method of claim 27, wherein the forming of the
16 plurality of conductive plugs comprises forming conductive material over
17 the insulative material over the conductive lines within the peripheral
18 area.

1 35. The method of claim 27, wherein the insulative material
2 comprises a first insulative material, and wherein:

3 the forming of the plurality of conductive plugs comprises forming
4 conductive material over the first insulative material over the conductive
5 lines within the peripheral area, and further comprising prior to the
6 removing of the first insulative material, forming capacitor container
7 openings over and exposing conductive plug portions within the memory
8 array.

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10 36. The method of claim 27, wherein the insulative material
11 comprises a first insulative material, and wherein:

12 the forming of the plurality of conductive plugs comprises forming
13 conductive material over the first insulative material over the conductive
14 lines within the peripheral area, and further comprising prior to the
15 removing of the first insulative material, forming both capacitor
16 container openings over and exposing conductive plug portions within the
17 memory array, and contact openings over conductive lines within the
18 peripheral area and exposing conductive material portions over the first
19 insulative material.

1 37. The method of claim 27, wherein the insulative material
2 comprises a first insulative material, and wherein:

3 the forming of the plurality of conductive plugs comprises forming
4 conductive material over the first insulative material over the conductive
5 lines within the peripheral area, and further comprising prior to the
6 removing of the first insulative material, forming both capacitor
7 container openings over and exposing conductive plug portions within the
8 memory array, and contact openings over conductive lines within the
9 peripheral area and exposing conductive material portions over the first
10 insulative material; and

11 forming a capacitor electrode layer within the capacitor container
12 openings and the contact openings.
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1 38. The method of claim 27, wherein the insulative material
2 comprises a first insulative material, and wherein:

3 the forming of the plurality of conductive plugs comprises forming
4 conductive material over the first insulative material over the conductive
5 lines within the peripheral area, and further comprising prior to the
6 removing of the first insulative material, forming capacitor container
7 openings over and exposing conductive plug portions within the memory
8 array; and

9 wherein the removing of the first insulative material comprises
10 using an etch chemistry effective to remove both conductive material
11 portions over the first insulative material and the first insulative
12 material.

13
14 39. A method of forming a dynamic random access memory
15 (DRAM) comprising:

16 forming a plurality of conductive plugs received over substrate
17 node locations over which storage capacitors are to be formed within
18 a memory array area; and

19 after the forming of the plugs, removing substantial portions of
20 individual conductive line insulative caps over and exposing conductive
21 material of conductive lines which are formed within a peripheral area
22 outward of the memory array area.

1 40. The method of claim 39 further comprising after the forming
2 of the plurality of conductive plugs:

3 forming an insulative material layer over the substrate; and

4 forming a plurality of openings received within the insulative
5 material layer, some of the openings comprising capacitor container
6 openings within which storage capacitors are to be formed, other of the
7 openings comprising first contact openings formed over the insulative
8 caps of the conductive lines within the peripheral area.

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10 41. The method of claim 39 further comprising after the forming
11 of the plurality of conductive plugs:

12 forming an insulative material layer over the substrate;

13 forming a plurality of openings received within the insulative
14 material layer, some of the openings comprising capacitor container
15 openings within which storage capacitors are to be formed, other of the
16 openings comprising first contact openings formed over the insulative
17 caps of the conductive lines within the peripheral area; and

18 forming a capacitor electrode layer within the capacitor container
19 openings and the first contact openings.
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1 42. The method of claim 39 further comprising after the forming
2 of the plurality of conductive plugs:

3 forming an insulative material layer over the substrate;

4 forming a plurality of openings received within the insulative
5 material layer, some of the openings comprising capacitor container
6 openings within which storage capacitors are to be formed, other of the
7 openings comprising first contact openings formed over the insulative
8 caps of the conductive lines within the peripheral area;

9 forming a pair of capacitor electrode layers within the capacitor
10 container openings and the first contact openings;

11 forming a patterned masking layer over the capacitor container
12 openings; and

13 removing unmasked portions of the pair of capacitor electrode
14 layers.

1 43. The method of claim 39 further comprising after the forming
2 of the plurality of conductive plugs:

3 forming an insulative material layer over the substrate;

4 forming a plurality of openings received within the insulative
5 material layer, some of the openings comprising capacitor container
6 openings within which storage capacitors are to be formed, other of the
7 openings comprising first contact openings formed over the insulative
8 caps of the conductive lines within the peripheral area;

9 forming a pair of capacitor electrode layers within the capacitor
10 container openings and the first contact openings;

11 forming a patterned masking layer over the capacitor container
12 openings; and

13 removing unmasked portions of the pair of capacitor electrode
14 layers, and wherein the removing of the substantial portions of the
15 individual conductive line insulative caps comprises removing said
16 portions with the patterned masking layer in place.

1 44. A method of forming a dynamic random access memory
2 (DRAM) comprising:

3 forming a plurality of conductive lines over a substrate having a
4 memory array area and a peripheral area outward of the memory array
5 area;

6 forming conductive material over the substrate comprising:

7 conductive plugs received over substrate node locations over
8 which storage capacitors are to be formed within the memory array
9 area, and

10 conductive material received over portions of some of the
11 conductive lines within the peripheral area;

12 forming openings through an insulative material and exposing the
13 conductive plugs within the memory array area and the conductive
14 material within the peripheral area;

15 forming a storage capacitor electrode layer within the openings;
16 and

17 removing portions of the storage capacitor electrode layer within
18 the memory array area and peripheral area sufficient to form a storage
19 capacitor electrode within the memory array and entirely remove the
20 storage capacitor electrode layer from within the peripheral area and
21 outwardly expose conductive portions of conductive lines within the
22 peripheral area.

1 45. The method of claim 44, wherein the forming of the storage
2 capacitor electrode layer comprises forming a cell plate layer within the
3 openings.

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5 46. The method of claim 44, wherein the forming of the storage
6 capacitor electrode layer comprises forming a cell plate layer within the
7 openings, and wherein the removing of the storage capacitor electrode
8 layer comprises doing so in a common masking step.

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10 47. The method of claim 44, wherein the forming of the storage
11 capacitor electrode layer comprises forming a cell plate layer within the
12 openings, and wherein the removing of the storage capacitor electrode
13 layer comprises doing so in a common etching step.

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15 48. The method of claim 44, wherein the forming of the storage
16 capacitor electrode layer comprises forming a storage node layer within
17 the openings.

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19 49. The method of claim 44, wherein the forming of the storage
20 capacitor electrode layer comprises forming a storage node layer within
21 the openings, and wherein the removing of the storage capacitor
22 electrode layer comprises doing so in multiple removing steps.